

CLAIMS

- Sub A1
1. A system configured to provide fast acknowledgement and efficient servicing of an interrupt issued to a processor of an intermediate node, the system comprising:
 - an external device coupled to a high latency path, the external device generating a pulsed interrupt signal for each type of interrupt supported by the processor;
 - an interrupt multiplexing device accessible by the processor over a fast bus, the interrupt multiplexing device adapted to issue the interrupt to the processor in response to each pulsed interrupt signal generated by the external device;
 - a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device; and
 - a status bit stored within the interrupt multiplexing device, the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device,
 - wherein the processor efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing device over the fast bus.
 2. The system of Claim 1 further comprising a current counter associated with the interrupt multiplexing device, the current counter incremented in response to each pulsed interrupt signal at the interrupt multiplexing device.
 3. The system of Claim 2 further comprising an interrupt handler invoked by the processor to service the issued interrupt.
 4. The system of Claim 3 further comprising a last counter associated with the processor, the last counter incremented in response to each interrupt serviced by the CPU.

1 5. The system of Claim 4 further comprising means for comparing a value of the last
2 counter with a value of the current counter to determine whether there are more interrupts
3 to service.

1 6. The system of Claim 5 wherein the means for comparing comprises the interrupt han-
2 dler.

1 7. The system of Claim 1 wherein the external device is a direct memory access con-
2 troller.

1 8. The system of Claim 1 wherein the low latency path is a printed circuit board trace.

1 9. The system of Claim 1 wherein the high latency path is a peripheral computer inter-
2 connect bus.

1 10. The system of Claim 1 wherein the interrupt multiplexing device is a field program-
2 mable gate array device.

1 11. A method for providing fast acknowledgement and efficient servicing of an interrupt
2 issued to a processor of an intermediate node, the method comprising the steps of:
3 generating a pulsed interrupt signal at an external device coupled to a high latency
4 path;
5 transporting the pulsed interrupt signal to an interrupt multiplexing device over a
6 low latency path coupling the external device to the interrupt multiplexing device;
7 asserting a status bit in response to detecting the pulsed interrupt signal at the in-
8 terrupt multiplexing device;
9 issuing the interrupt to the processor in response to each pulsed interrupt signal
10 received at the interrupt multiplexing device; and
11 invoking an interrupt handler to service the issued interrupt.

1 12. The method of Claim 11 further comprising the step of initializing a last counter.

1 13. The method of Claim 12 further comprising the steps of:

2 reading the status bit; and

3 if the status bit is clear, dismissing the handler.

1 14. The method of Claim 13 wherein the step of reading further comprises the step of
2 clearing the status bit.

1 15. The method of Claim 13 further comprising the steps of:

2 if the status bit is set, reading a value of a current counter;

3 comparing the current counter value with a value of the last counter; and

4 if the last counter value is greater than or equal to the current counter value, re-
5 turning to the step of reading the status bit.

1 16. The method of Claim 15 further comprising the steps of:

2 if the last counter value is not greater than or equal to the current counter value,
3 checking a control block stored in a memory of the node, the control block shared be-
4 tween the processor and the external device; and

5 determining whether the processor owns the control block.

1 17. The method of Claim 16 further comprising the steps of:

2 if the processor owns the control block, processing the control block; and

3 incrementing the last counter.

1 18. The method of Claim 17 further comprising the steps of:

2 determining whether a preset limit for processing control blocks has been
3 reached; and

4 if the preset limit is reached, dismissing the handler.

1 19. Apparatus for providing fast acknowledgement and efficient servicing of an inter-
2 rupt issued to a processor of an intermediate node, the apparatus comprising:

3 means for generating a pulsed interrupt signal at an external device coupled to a
4 high latency path;

5 means for transporting the pulsed interrupt signal to an interrupt multiplexing de-
6 vice over a low latency path coupling the external device to the interrupt multiplexing
7 device;

8 means for asserting a status bit in response to detecting the pulsed interrupt signal
9 at the interrupt multiplexing device;

10 means for issuing the interrupt to the processor in response to each pulsed inter-
11 rupt signal received at the interrupt multiplexing device; and

12 means for invoking an interrupt handler to service the issued interrupt.

1 20. A computer readable medium containing executable program instructions for pro-
2 viding fast acknowledgement and efficient servicing of an interrupt issued to a processor
3 of an intermediate node, the executable program instructions comprising program in-
4 structions for:

5 generating a pulsed interrupt signal at an external device coupled to a high latency
6 path;

7 transporting the pulsed interrupt signal to an interrupt multiplexing device over a
8 low latency path coupling the external device to the interrupt multiplexing device;

9 asserting a status bit in response to detecting the pulsed interrupt signal at the in-
10 terrupt multiplexing device;

11 issuing the interrupt to the processor in response to each pulsed interrupt signal
12 received at the interrupt multiplexing device; and

13 invoking an interrupt handler to service the issued interrupt.

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